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Dedicated Computational Models for the Electromagnetic Emissions of Integrated Circuits

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Abstract — **To model the electromagnetic emissions of integrated circuits, a full chip simulation is the most accurate method. Full chip simulations are very complex, time consuming, and do not protect the intellectual property. Therefore, other models were developed that are fast, protect confidential information and have a lower complexity. In this paper, we give a state-of-the-art overview of these models.**

1 INTRODUCTION

The manufacturers of all electronic devices are obligated to develop their products according to the electromagnetic compatibility (EMC) requirements. The current EMC standards basically only set limits for the final products and not for its subcomponents [1]. As a consequence, the first EMC tests are often postponed until very late in the design process when a first complete prototype system is available, leading to a high cost and delay if the device does not pass the EMC test. Therefore, electromagnetic (EM) emission estimations of subcomponents concerning EMC are necessary at the design level.

Nowadays, due to the increasing complexity, operating frequencies, bitrates and miniaturization of microelectronic components, emissions from integrated circuits (ICs) have gained importance [2]. Indeed, this miniaturization leads to faster and stronger current peaks by the simultaneous switching of millions of transistors. These transient currents leave the IC through silicon paths, bonding wires, and the package lead frame. They further propagate through the PCB tracks that may act as unwanted antennas, and flow to other semiconductor devices, potentially disrupting their normal operation [3]. Consequently, it is necessary that the design engineer can characterize the emissions from the ICs already early in the design process. This can be done by EMC simulation models which predict the conducted and/or radiated emissions from the IC. Of course, this can also be done by full chip simulation, but these methods are time consuming and expose intellectual property. Therefore, several nonconfidential models have been proposed for describing the EMC behavior of an IC. In this paper, we give a state-of-the-art overview of these models.

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2 DESCRIPTION OF THE AVAILABLE MODELS

2.1 IBIS

The first significant contribution to the EMC modeling of components came from the input/output buffer information specification (IBIS). It was initiated by Intel Corporation in the early 1990s and has nowadays achieved wide spread international support and recognition [5]. This standard gives specifications for the electrical performance of the input/output structures of an IC up to a frequency of 1 GHz [4].

IBIS is a so-called behavioral simulator as opposed to circuit simulators and EM simulators. A circuit simulator (e.g., SPICE) solves differential equations corresponding to various circuit elements to predict the current and voltage at different nodes within the circuit. An EM simulator solves the Maxwell equations and evaluates electric and magnetic fields at different locations. These two simulation methods are very accurate but computationally slow. Behavioral simulators, on the other hand, use a set of tables to obtain voltages and currents. This results in the advantage that behavioral simulators are accurate and computationally faster than circuit and EM simulators [6]. These tables and other information in the IBIS models are written in a human readable ASCII text based format. They contain non-linear electrical characteristics of the input and output pins of a component. In other words, they ignore the internal behavior of the components and consider them as black boxes. They only model the behavior at the terminals. Because they do not include transistor-level implementation details, they preserve intellectual property and are computationally very fast. Since they describe in a nonconfidential way the electrical performance of the I/O structures of an IC, the IBIS model can be re-used in different designs. The model can also be used at an early stage of the design process as there

is no need for circuit specifications [6]. Although the key concepts of the IBIS model are simple, the details are very complex, which makes it important to rigorously follow the processes and software tools for making and validating IBIS data model files [7].

Two types of data elements make up the bulk of the data entries of an IBIS data file. (i) A current-voltage lookup table for its dynamic, non-linear impedance behavior: at a given voltage, the lookup table returns a current. Ohm's law is implicitly "solved", but since the resistance is non-linear, the data is stored as an I-V lookup table. Both input and output impedances are needed [7]. (ii) A ramp voltage-time lookup table for its dynamic, non-linear switching signal behavior: at a given time, the lookup table returns a voltage. This is equivalent to the description of the time domain output waveform of a generator [7].

The IBIS model provides that a component (the black box) connected to an I/O pin can be enabled either as an output or as an input, depending on what is present in the physical device, pin use, and user instructions [7]. The data in the lookup tables is either generated by simulation from a company's proprietary model or is generated by direct measurement of behavior at the pins of the component. Unfortunately, the IBIS model has several imperfections [2][3][8]. (i) It does not take into account the main source of IC parasitic emissions, i.e., the high-frequency currents induced in the IC supply current by the simultaneous switching noise. (ii) The modeling of power and ground currents is insufficient for accurate power and ground bounce analysis. (iii) Since the IBIS model has only the final stage at output and input, it is difficult to model the effect of loading of circuit boards on output and input waveforms. (iv) In order to model EM emissions with more accuracy, more information such as material constant and three-dimensional structures is needed.

2.2 LECCS

The linear equivalent circuit and current source (LECCS) model is an electrical model originally proposed as an immunity model for core circuits of ICs and large-scale integration. The first version (the LECCS-core model) was proposed to evaluate the radio frequency noise current on a power pin of a core logic circuit [9] and was then extended to a model for devices that have output drivers (the LECCS-I/O model) [10].

The LECCS model is defined in the frequency domain and consists of an equivalent internal impedance of the IC and an equivalent internal current source that expresses the internal noise source caused by the switching operations of transistors [11]. It is able to predict the conducted emissions and analyze the immunity up to 1 GHz [2].

An equivalent circuit for averaged circuit states of CMOS can be represented by a parallel circuit of an RC-chain and an equivalent internal current source. The values R and C are, respectively, the on-resistance and the capacitance between drain and source [11]. And since the functional blocks of ICs consist of CMOS transistors, the approximated equivalent circuit model of an IC can be described by an RLC-series circuit in parallel with an equivalent internal current source. The internal current I_i can be calculated with:

$$I_i = \frac{Z_i + Z_s}{Z_i} I_v, \tag{1}$$

with Z_i the synthesized circuit impedance of the equivalent circuit, Z_s the measured or simulated internal impedance of the power supply and I_v the measured power current [11].

The LECCS model has the following features [9]. (i) All the model parameters can be determined by measurements. It is therefore not necessary to take the internal design parameters into account. Of course, one can also derive the parameters from simulation, for example with a SPICE model, for the internal components. (ii) The internal current source can be determined from the measured current spectrum. (iii) The model can express the noise characteristics of the power current of an IC. The effects of e.g., the decoupling capacitors on a PCB or of on-package and on-chip decoupling capacitors can be evaluated. (iv) Although the model is linear and has a very simple structure, its accuracy is sufficient for the simulation of EM emissions. Of course, transistors have nonlinear switching characteristics. Their impedance varies in accordance with their evolution of switching operation. However, most of the noise characteristics are related to certain resonance phenomena of the PCB and device impedances, and most of the noise appears as a combination of damped oscillations. The switching duration of each transistor is short, compared to the time constants of the noise current. Therefore, most of the noise emissions of an IC can be expressed by a linear macro-model [5].

2.3 IMIC

In order to ameliorate the IBIS model described above, the interface model for ICs (IMIC) was developed, which takes more phenomena into account as for example the ground and power supply pin bounce. IMIC standardizes the electrical modeling of input signals, output signals, power supply,

and ground terminals of ICs, in order to enable the analysis of electric characteristics of equipment using them. The details are described in the standard IEC 62404 [8] for frequencies up to 1 GHz. IMIC has a hierarchical model structure. It has 3 levels of models: the module models, the IC models and the package models. Those 3 models are described in a unified way. In the simulation, the module model refers to the IC models and optionally to other module models. The IC model refers to the package model. Due to this hierarchical structure, users can easily recognize pins and signals at which they aim, because outer terminals and signals of each model are clearly defined in each model. Moreover, IC and package makers can provide IC and package models, respectively, because each model is independent from each other except for the part that defines their relationships [5].

A better accuracy than the IBIS model can only be achieved by disclosing -to some extent- proprietary information of the IC. However, two mechanisms are built in IMIC to greatly reduce the disclosure of proprietary information of process parameters. Firstly, IMIC allows that waveforms can be defined and be assigned to circuit nodes. And secondly, the non-linear devices are modeled using a tabular text format that consists of sets of parameters that are either independent variables (terminal voltages) or dependent variables (currents and capacitances) [5].

2.4 ICEM

Nowadays, the most common used EMC model is the integrated circuit electromagnetic model (ICEM), which has been standardized within the IEC standard 62014-3 [12]. The model can be used for emission simulations due to IC internal activities, within the frequency range of 150 kHz to 1 GHz [2]. It allows IC manufacturers and system integrators to analyze, optimize, and predict several parameters such as auto compatibility of mixed-signal ICs, radiated and conducted emissions of an IC, radiated emission of a global system, decoupling capacitors on a printed circuit board (PCB) and the number of power-supply pin pairs [13][14]. The purpose of this standard model is to provide data to enable PCB EM tools to compute the EM fields produced by ICs and their associated PCB. These data can be extracted from measurement methods or obtained from IC simulation tools [12]. It gives accurately the EM emissions of electronic equipment by taking into account the influence of internal activities. Mainly for this reason, it has to a certain extent replaced the IMIC and IBIS model, which are focused on interface activity predictions (cross-talk, overshoot, ..) [12]. We want to note that IBIS made it possible to link its data to the ICEM model.

The main advantage of the ICEM model is the reduction of the complexity of the IC. By doing so, the IC can be simulated on a basic analog simulator such as SPICE, allowing the design engineer to evaluate the noise values in an early stage of the design process [14].

The basic architecture of the ICEM model is composed of two submodels [14]. The first is the Internal Activity (IA) submodel which describes the internal currents flowing in the IC. It resumes the contribution of all the internal blocks (analog, digital and I/O structures) on the current circulating between the power supply pins of the IC [15]. Typically, the IA submodel is a current source that can either be expressed in the time domain or in the frequency domain. One can use a standard waveform, a simulation file or a measurement result (described as a piece-wise function) for the current source [3]. The second submodel, the Passive Distribution Network (PDN) submodel, describes the passive electrical structure for powering the internal functions integrated on the chip. It corresponds to the impedance network seen between the power supply and ground pins [3]. They can be represented by either lumped electrical elements such as resistance, inductance and capacitance or transmission-line models [13]. These passive elements are determined by contributions from as well the component (junction capacitance, oxide capacitance, metal capacitance, interconnection resistance and inductance) as the package (resistance and capacitance of the leads, the bonding, capacitance between the pins of the package) [15]. There are two ways to generate these sub-models. The first method is used during the design phase and allows to have the ICEM at the early stage of the design cycle. It uses IC design tools to evaluate the impedance of the power network of the die and to rebuild the current consumed by the digital parts. The second approach uses measurement tools such as a network analyser, a time domain reflectometer, a scope or a fast Fourier transform process. It relies on these measurements in order to extract the impedance of the power network and the internal current consumed on the die [14][15].

This basic ICEM model can be extended with a substrate network model in order to take substrate effects into account. It consists of an *RC* network that models the substrate voltages and currents propagation [16]. Notice that the structure of ICEM is very similar to that of the LECCS model.

Although ICEM has been revealed as an excel-

lent model to predict the emissions, it is limited in frequencies up to 1 GHz. Moreover, ICEM models the EM noise of an IC as a current source, described as an ASCII text file or a triangular waveform. By modeling the internal activity with an ASCII file, it is difficult to quantify its variation. On the other hand, it is difficult to achieve a good correlation between the IA model and the IA measurement with a triangular waveform. Therefore, an electrical model was recently presented for characterizing and modeling the conducted emissions of an IC up to 3 GHz [2].

3 CONCLUSION

To model the EM emissions of ICs, a full chip simulation is the most accurate method. However, full chip simulation is very complex and time consuming. Moreover, the intellectual property is not protected. Therefore, other models were developed that are fast, protect confidential information and have a medium (IBIS) or low (LECCS, IMIC, ICEM) complexity [1]. Moreover, the accuracy for the calculated EM emissions from these models is usually sufficient for practical EMC applications. An important drawback of these models is their limited frequency range (up to 1 GHz), although adaptations for higher frequencies exist [2]. We emphasize that nowadays, IBIS and ICEM are the most wide spread accepted models.

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